WHAT IS CLAIMED IS:

1. A processor comprising:

a segment register having a portion for storing a segment base address;

a register for storing an address; and

an execution core coupled to the segment register and the register, wherein the execution core is configured, in response to a first instruction, to swap the segment base address in the segment register and the address in the register.

2. The processor as recited in claim 1 wherein the register is a special purpose register.

3. The processor as recited in claim 1 wherein the register is a model specific register.

4. The processor as recited in claim 1 wherein each of the segment base address and the address include greater than 32 bits.

5. The processor as recited in claim 4 wherein the execution core is coupled to receive an indication of an operating mode of the processor, and wherein the operating mode specifies a default address size, and wherein the execution core is configured to execute the first instruction if the default address size is greater than 32 bits.

6. The processor as recited in claim 5 wherein the execution core is configured to signal an exception if the default address size is not greater than 32 bits.

7. The processor as recited in claim 1 wherein the first instruction is privileged.

8. The processor as recited in claim 7 wherein the execution core is configured, responsive to one or more predefined instructions separate from the first instruction, to read or write the register, and wherein the one or more predefined instructions are also privileged.

9. The processor as recited in claim 8 wherein the execution core is configured, responsive to the one or more predefined instructions or the first instruction, to signal an exception if a privilege level of the processor is not sufficient for execution of the one or more predefined instructions or the first instruction.

10. An apparatus comprising:

a first storage location corresponding to a segment register, the first storage location having a portion for storing a segment base address;

a second storage location corresponding to a register, the second storage location for storing an address; and

a processor coupled to the first storage location and to the second storage location, wherein the processor is configured, in response to a first instruction, to swap the segment base address in the first storage location and the and the address in the second storage location.

11. The apparatus as recited in claim 10 wherein the register is a special purpose register.

12. The apparatus as recited in claim 10 wherein the register is a model specific register.

13. The apparatus as recited in claim 10 wherein each of the segment base address and

the address include greater than 32 bits.

14. The apparatus as recited in claim 13 wherein the processor, in response to an operating mode specifying a default address size, is configured to process the first instruction if the default address size is greater than 32 bits.

15. The apparatus as recited in claim 14 wherein the processor is configured to signal an exception if the default address size is not greater than 32 bits.

16. The apparatus as recited in claim 10 wherein the first instruction is privileged.

17. The apparatus as recited in claim 16 wherein the processor is configured, responsive to the first instruction, to signal an exception if a privilege level is not sufficient for execution of the first instruction.

18. A carrier medium holding an instruction which, when executed, causes a segment base address from a segment register and an address stored in a different register to be swapped.

19. The carrier medium as recited in claim 18 wherein the different register is a special purpose register.

20. The carrier medium as recited in claim 18 wherein the different register is a model specific register.

21. The carrier medium as recited in claim 18 wherein the instruction is privileged and wherein the instruction, when executed, causes an exception if a privilege level of the executing processor is insufficient to execute the instruction.

22. The carrier medium as recited in claim 18 wherein each of the segment base address and the address include greater than 32 bits, and wherein the instruction, when executed, causes an exception if the operating mode of the executing processor does not specify an address size greater than 32 bits.

23. A carrier medium configured to hold an operating system routine including a first instruction which, when executed, causes a segment base address from a segment register and a base address stored in a register to be swapped, wherein the base address stored in the register is a pointer to one or more operating system data structures.

24. The carrier medium as recited in claim 23 wherein the operating system routine further includes one or more instructions which, when executed, save a first stack pointer from a stack pointer register to one of the one or more operating system data structures.

25. The carrier medium as recited in claim 24 wherein the operating system routine further includes one or more instructions which, when executed, load a second stack pointer into the stack pointer register from the one or more operating system data structures, the second stack pointer indicating a stack used by the operating system routine.

26. The carrier medium as recited in claim 23 wherein the operating system routine includes one or more instructions which, when executed, perform an operating system service.

27. The carrier medium as recited in claim 26 wherein the operating system routine further includes a second instruction subsequent to the one or more instructions, the second instruction, when executed, causing a swap of the segment base address from the segment register and the base address stored in the register to be swapped, thereby restoring a state of the segment register and the register to the state prior to the execution

of the first instruction.

28. The carrier medium as recited in claim 27 wherein the first instruction and the second instruction have the same binary coding.

29. The carrier medium as recited in claim 23 wherein the first instruction is an initial instruction of the operating system routine.

30. A processor comprising:

a special purpose register for storing a first address;

a register for storing a second address; and

an execution core coupled to the special purpose register and the register, wherein the execution core is configured, in response to a first instruction, to swap the first address in the special purpose register and the second address in the register.